

User Guide

*SIB064
64 Channel PMT Interface Board
Hamamatsu H8500D series*



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General Safety Precautions

Use Proper Power Source

The SIB064 is powered with a +5V power source directly from Vertilon's PhotoniQ multi-channel data acquisition systems. Use with any other power source may result in damage to the product.

Operate Inputs within Specified Range

To avoid electric shock, fire hazard, or damage to the product, do not apply a voltage to any input outside of its specified range.

Electrostatic Discharge Sensitive

Electrostatic discharges may result in damage to the SIB064. For these reasons, the SIB064 board is intended to be operated in a user's conductive instrument enclosure.

Do Not Operate in Wet or Damp Conditions

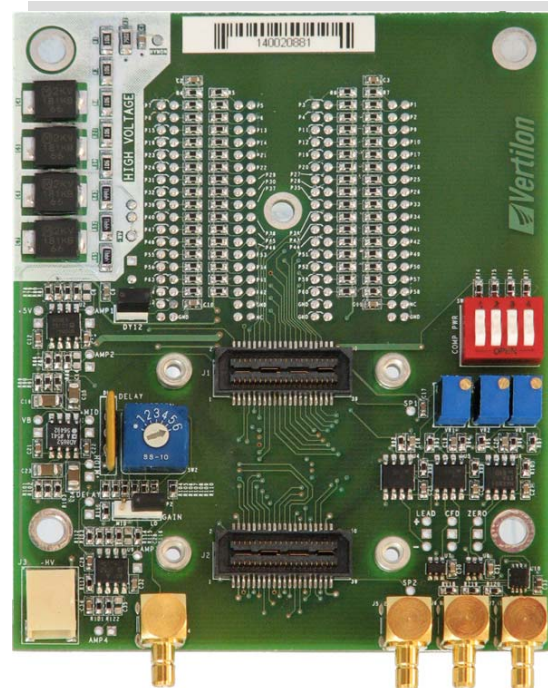
To avoid electric shock or damage to the product, do not operate in wet or damp conditions.

Do Not Operate in Explosive Atmosphere

To avoid injury or fire hazard, do not operate in an explosive atmosphere.

Product Overview

- Mounting board for Hamamatsu H8500D 64 channel MAPMT
- Provides 64 channel interface to data acquisition systems
- Separate high voltage input for PMT cathode bias
- High speed preamplifier for last dynode output
- Leading edge, constant fraction, and zero slope discriminators
- Adjustable gain and discriminator thresholds
- 100% compatible with Vertilon's PhotoniQ multichannel DAQs
- No external power supply required



The SIB064 multianode photomultiplier tube interface board provides the mechanical and electrical connectivity between the Hamamatsu H8500D 64 anode PMT and external signal processing electronics such as Vertilon's PhotoniQ multichannel data acquisition systems. The H8500D is mounted to the bottom side of the SIB064 through 148 socket pins that connect the PMT's 64 anode signals, high voltage input, and last dynode output to the board. The anode signals are routed to two connectors located on the top of the board that each connect to a specialized high density coaxial cable assembly. This arrangement allows the SIB064 to be conveniently mounted directly into the user's optical setup with the PMT facing outward from the bottom of the board and the sensor interface board (SIB) cables exiting from the top. The SIB cables carry the 64 anodes from the H8500D to the PhotoniQ where the charge from each is separately integrated, digitized, and sent to a PC for display or further signal processing. The negative high voltage bias to the PMT's cathode is supplied directly from the PhotoniQ on a high voltage cable to a dedicated connector on the SIB064. For applications utilizing the last dynode output of the H8500D, the SIB064 includes a two stage high speed preamplifier whose output is available on an SMB connector. When critical timing and triggering are required, this output can be connected to a separate high performance external discriminator. Alternatively, one of the three on-board discriminators can be used when the timing requirements are not as stringent. The outputs from a leading edge, constant fraction, and zero slope discriminator — which respectively generate trigger signals based on a threshold, percentage of pulse height, and pulse peak — are each available on an SMB connector. Several user adjustments are included for optimizing system gain and trigger thresholds for the discriminators.

The various functions on the SIB064 are described in greater detail on the following pages. When necessary, refer to the functional block diagram shown in Figure 1 below.

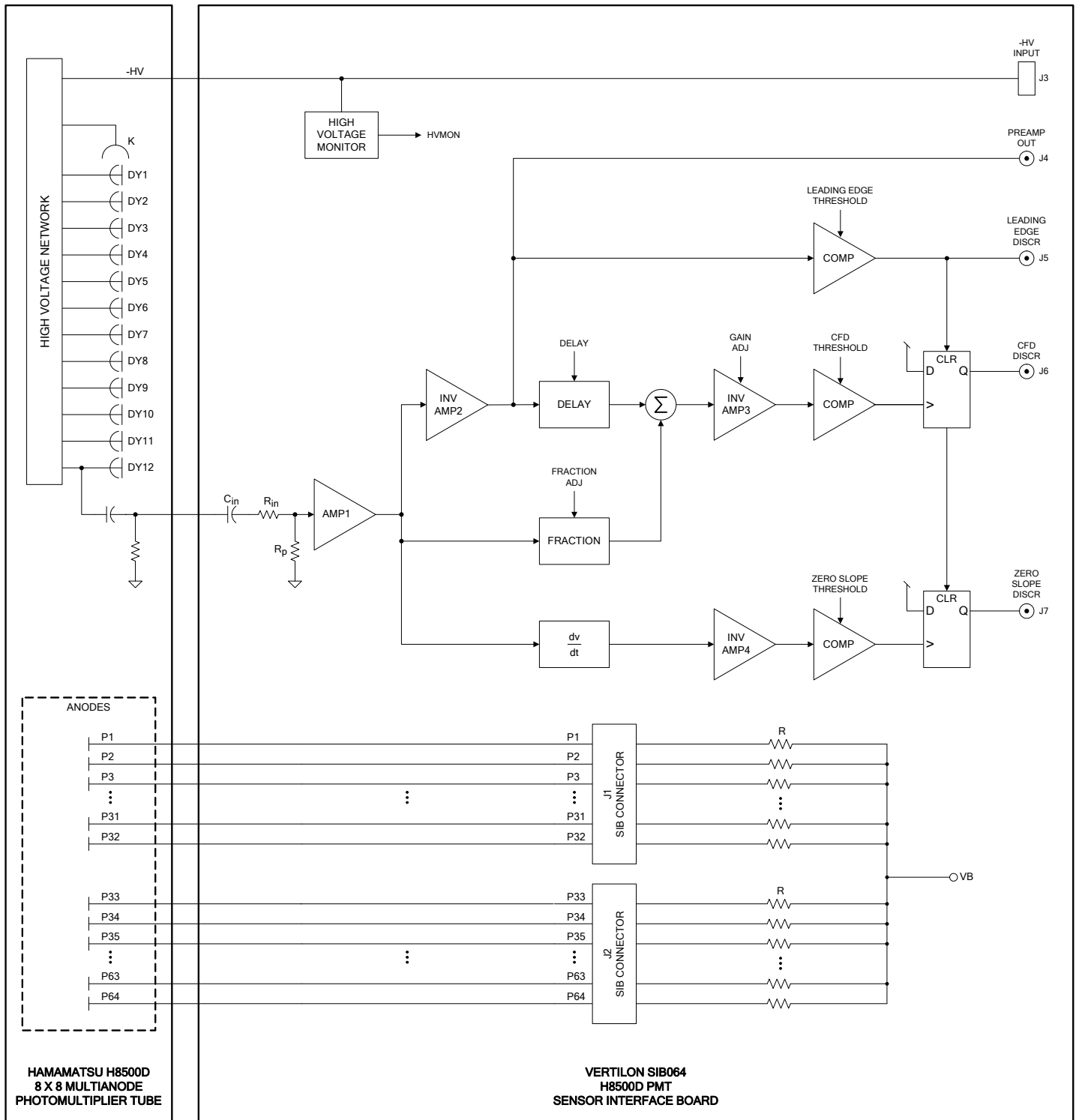


Figure 1: Functional Block Diagram

Specifications

($V_{\text{supply}} = +5.0\text{V}$, $T_A = +25\text{C}$, unless otherwise noted)

Description	Sym	Min	Typ	Max	Units	Notes
HIGH VOLTAGE						
High Voltage Input Load Resistance			50		M Ω	Measured at high voltage input connector, J3
HVMON to High Voltage Input Ratio			0.0015			$\pm 20\%$
ANODE CIRCUITS						
Quantity	P1 - P64		64			
Input Resistance	R		2.2		M Ω	
Input Bias Voltage	VB		+0.250		V	Detector bias voltage supplied from PhotorIQ data acquisition system
LAST DYNODE PREAMPLIFIER						
Input Coupling Capacitance	C_{in}		0.1		μF	
Input Resistance	R_{in}		50		Ω	
Input Parallel Resistance	R_{p}		500		Ω	
Amplifier #1 Gain	A1		12.6		dB	
Amplifier #2 Inverting Gain	A2		6		dB	V_{in} is a triangular pulse (18 nsec rise time, 30 nsec fall time) applied to last dynode preamplifier input (DY12).
Amplifier #2 Output Impedance			50		Ω	Measured at preamplifier output, J4
LEADING EDGE DISCRIMINATOR						
Threshold Adjustment	V_{th1}	-25		0	mV	Referenced to baseline level at comparator input
Threshold to Output Delay ($V_{\text{in}}=30\text{mV}$)	t_{d1}		5		nsec	
Time Walk (V_{in} : 3mV to 30mV)			-13		nsec	Output on connector, J5.
Time Walk (V_{in} : 30mV to 150mV)			-3.0		nsec	V_{in} is a triangular pulse (18 nsec rise time, 30 nsec fall time) applied to last dynode preamplifier input (DY12). Threshold (V_{th1}) set to 15mV below the baseline.
Jitter (V_{in} : 10mV)			500		psec	
CONSTANT FRACTION DISCRIMINATOR						
Delay	D		5		nsec	Standard delay element, other delays available.
Delay to Fraction Ratio		0.12		0.50		7 steps of 2 dB each Steps: 0.12, 0.16, 0.20, 0.25, 0.31, 0.40, 0.50
Amplifier #3 Inverting Gain	A3		+8.6		dB	
Threshold Adjustment	V_{th2}	0		+25	mV	Referenced to baseline level at comparator input
Threshold to Output Delay ($V_{\text{in}}=30\text{mV}$)	t_{d2}		6		nsec	Output on connector, J6.
Time Walk (V_{in} : 10mV to 100mV)			-0.8		nsec	V_{in} is a triangular pulse (18 nsec rise time, 30 nsec fall time) applied to last dynode preamplifier input (DY12). Threshold (V_{th2}) set to 15mV above the baseline. Fraction set to 0.50.
Jitter (V_{in} : 50mV)			500		psec	

Description	Sym	Min	Typ	Max	Units	Notes
ZERO SLOPE DISCRIMINATOR						
Differentiator First-Order Time Constant			3.3		nsec	
Amplifier #4 Inverting Gain	A4		10.4		dB	
Threshold Adjustment	V _{th3}	0		+25	mV	Referenced to baseline level at comparator input
Threshold to Output Delay (V _{in} =30mV)	t _{d3}		6		nsec	Output on connector, J7.
Time Walk (V _{in} : 20mV to 200mV)			-1.5		nsec	V _{in} is a triangular pulse (18 nsec rise time, 30 nsec fall time) applied to last dynode preamplifier input (DY12). Threshold (V _{th3}) set to 5mV above the baseline.
Jitter (V _{in} : 100mV)			500		psec	
DISCRIMINATOR OUTPUTS						
Output Impedance			50		Ω	
Logic High Output Level	V _{OH}	+4.3	+4.8		V	(I _{OH} = -32mA)
Logic Low Output Level	V _{OL}		+0.2	+0.6	V	(I _{OL} = 32mA)
POWER						
Supply Voltage	V _{supply}	+4.9	+5.0	+5.1	V	
Supply Current	I _{supply}		75		mA	(all comparators enabled)
Supply Current	I _{supply}		55		mA	(all comparators disabled)
DIMENSIONS						
Width	W		84		mm	
Length	L		102		mm	(not including SMB connectors which extend past PCB edge)
Thickness	T		2.5		mm	(printed circuit board only)

Table 1: Specifications

Typical Setup

A typical setup using a SIB064 is shown below. The Hamamatsu H8500D PMT is mounted to the SIB064 and positioned to detect incoming light from a scintillator crystal or optical assembly. Two SIB cables connect the 64 anode outputs from the SIB064 to a PhotoniQ IQSP482 or IQSP582 64 channel PMT data acquisition system. Through a USB 2.0 connection the digitized output data from the PhotoniQ is sent to a PC for display, logging, or real time processing. Additional connections between the SIB064 and PhotoniQ include a high voltage cable that provides up to 1400 volts of negative bias to the H8500D cathode, and a trigger cable that supplies the trigger to the PhotoniQ from one of the SIB064's three discriminators. In an alternative configuration when precision timing is required, an external discriminator can be placed between the SIB064 preamplifier output and the PhotoniQ trigger input.

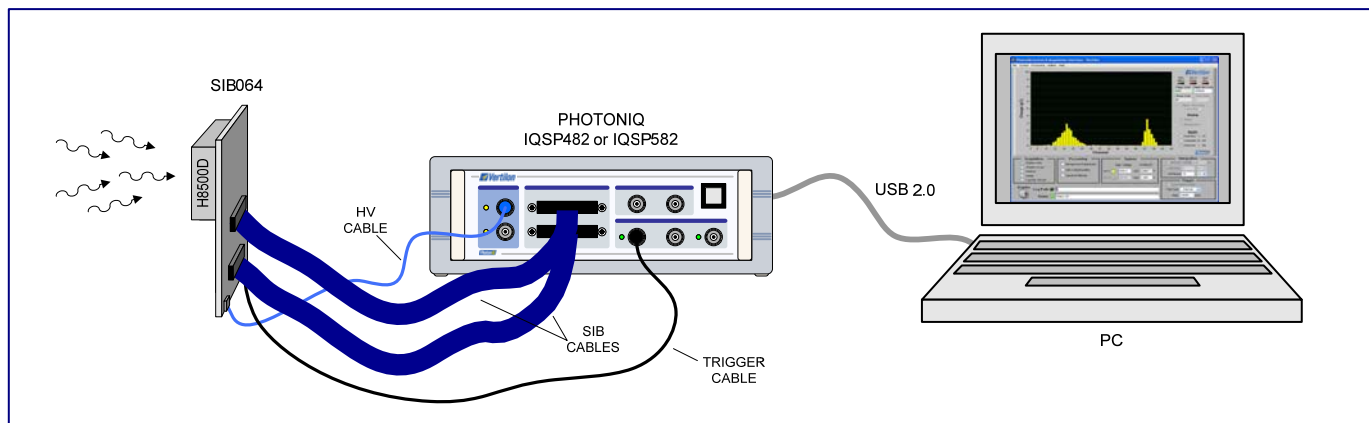


Figure 2: Typical Setup

High Voltage Interface

The SIB064 employs the interface circuit shown below between the high voltage input connector, J3, and the high voltage input to the H8500D. The monitor output (HVMON) allows the high voltage cathode bias for the PMT to be indirectly monitored at a reduced voltage level. Voltage readings at the monitor point should be scaled by a factor of 667. Calibration of the scale factor may be required.

Warning: The high voltage section of the SIB064 contains signals at voltage levels that can exceed negative 1500 volts. Never touch a component or signal in this area.

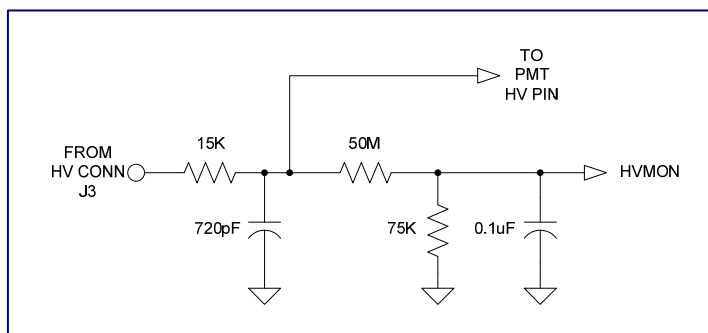


Figure 3: PMT High Voltage Interface Circuit

Photomultiplier Tube Anode Circuits

The 64 anode signals (P1 – P64) from the H8500D PMT are routed directly on the SIB064 to two specialized connectors referred to as sensor interface board (SIB) connectors. Anodes P1 to P32 route to SIB connector J1 and anodes P33 to P64 route to SIB connector J2. Each SIB connector mates to a proprietary low-noise, high density SIB cable assembly that carries the 32 anode signals on coaxial connections to a Vertilon PhotoniQ 64 channel PMT data acquisition system. Depending on the required speed and dynamic range, either a PhotoniQ IQSP482 high dynamic range system or an IQSP582 high speed system can be used as the main data acquisition unit. To minimize the possibility of damage due to ESD, the H8500D anodes each have a 2.2 Mohm shunt resistor to a common low impedance point. This point is biased at a voltage equal to the bias voltage (VB) of the charge integrating transimpedance amplifiers on the PhotoniQ so that the anodes can be DC coupled to them. Figure 4 below illustrates the equivalent circuit as seen by each PMT anode.

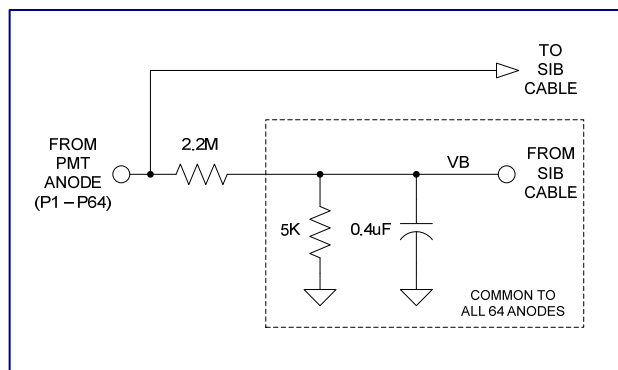


Figure 4: Anode Circuit

Last Dynode Preamp

This last dynode preamp is an inverting, AC-coupled, two-stage configuration whose input is designed for small positive voltage pulses from the last dynode (DY12) of the H8500D. The preamp's output can be further processed by three different discriminators on the SIB064 to generate trigger signals in sync with the pulse on the last dynode. For specialized applications requiring external discrimination of the last dynode signal, the preamp output is available on SMB connector, J4. The preamp should be disconnected from the PMT by removing jumper JP1 when the last dynode signal is unused.

Leading Edge Discriminator

The leading edge discriminator is a simple timing circuit that generates a trigger signal when a charge pulse on the last dynode output from the H8500D PMT exceeds a user-defined threshold. It is implemented using a high speed comparator connected to the output of the last dynode preamp. Referring to Figure 5, negative going pulses from the preamp are compared to a threshold that is adjusted using the "LEAD" potentiometer on the SIB064. A logic high is generated on the comparator output (SMB connector, J5) after a small delay (t_{d1}) from when the pulse first crosses the threshold, V_{th1} . The comparator switches back to a logic low when the pulse crosses the threshold from the opposite direction as it returns back to the baseline level. Because the trigger point is sensitive to the pulse height, this discriminator is typically used in applications that do not require precision timing. When not used, the leading edge discriminator should be disabled by switching switch SW1-1 to the "OPEN" position.

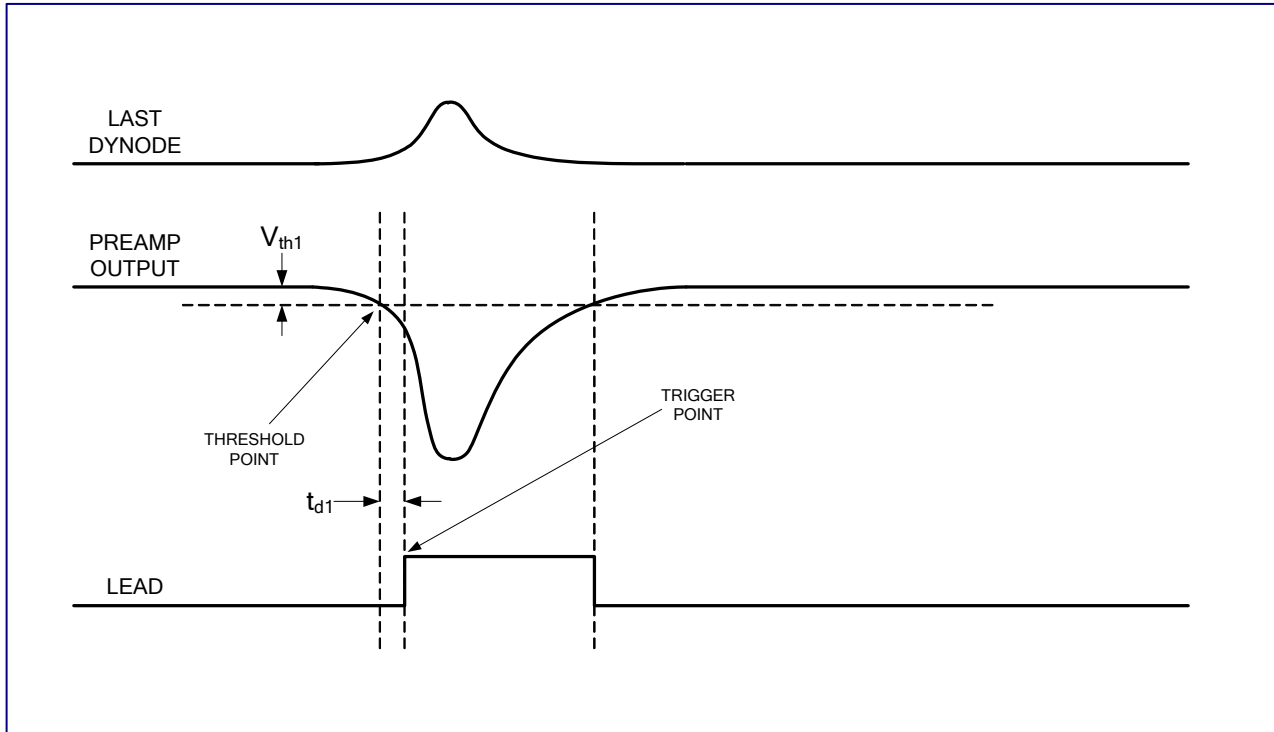


Figure 5: Leading Edge Discriminator Timing

Constant Fraction Discriminator

Unlike leading edge discriminators, a constant fraction discriminator (CFD) is capable of generating precisely timed trigger signals that are relatively independent of input pulse height. The CFD accomplishes this by subtracting a fraction of the input from a delayed version of the input such that the resulting signal always crosses zero at exactly the same point in time. To minimize triggering on noise, the threshold is set just above the zero crossing point. The timing diagram in Figure 6 below illustrates the technique as implemented on the SIB064. The CFD operates on the output of the last dynode preamplifier although technically only the delayed version of the signal (DELAY) is taken from the preamplifier output — the fractional part (FRACTION) is derived from the output of the first stage. The sum of these two components results in the AMP3 signal which is fed directly to the threshold comparator. This comparator, which to minimize noise triggering is only enabled when the output of the leading edge discriminator is high, compares AMP3 to a user-adjustable threshold voltage (V_{th2}) to generate the CFD output signal. By adjusting the delay time, fraction, and threshold (V_{th2}), the CFD can be made to trigger at any reasonable percentage of the pulse height maximum. The SIB064 ships with a standard fixed delay of 5 nsec (other delays of up to 10 nsec can be ordered separately) and seven preset fractions from 0.12 to 0.50 that are selectable using an on-board micro-rotary switch (SW2). The trigger threshold is adjusted using the "CFD" potentiometer. The leading edge discriminator must be enabled when using the CFD. When not used, the CFD can be disabled by switching switch SW1-2 to the "OPEN" position.

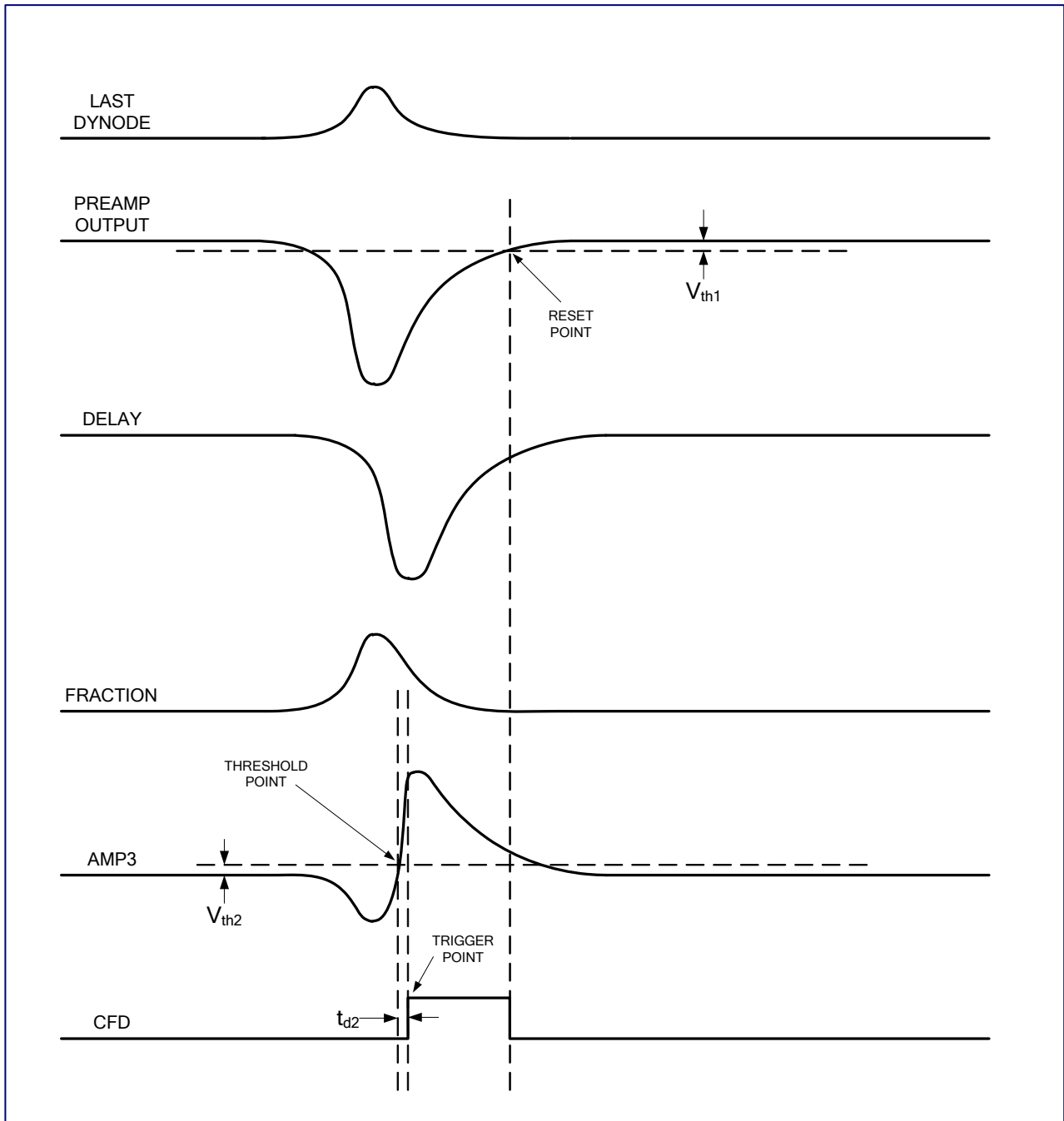


Figure 6: Constant Fraction Discriminator Timing

Zero Slope Discriminator

The zero slope discriminator works by generating a trigger signal at the inflection point of the input pulse. It is this point where the pulse is at its peak and its slope transitions from positive to negative. Since AMP4 effectively operates on the derivative of the input pulse, its output crosses zero where the slope of the pulse is zero. This occurs at the pulse peak as shown in Figure 7. The threshold comparator compares AMP4 to the user-adjustable threshold (V_{th3}) to generate the trigger signal. Similar to the constant fraction discriminator, the comparator is only enabled when the output of the leading edge discriminator is high. The zero slope discriminator is disabled by switching switch SW1-3 to the "OPEN" position.

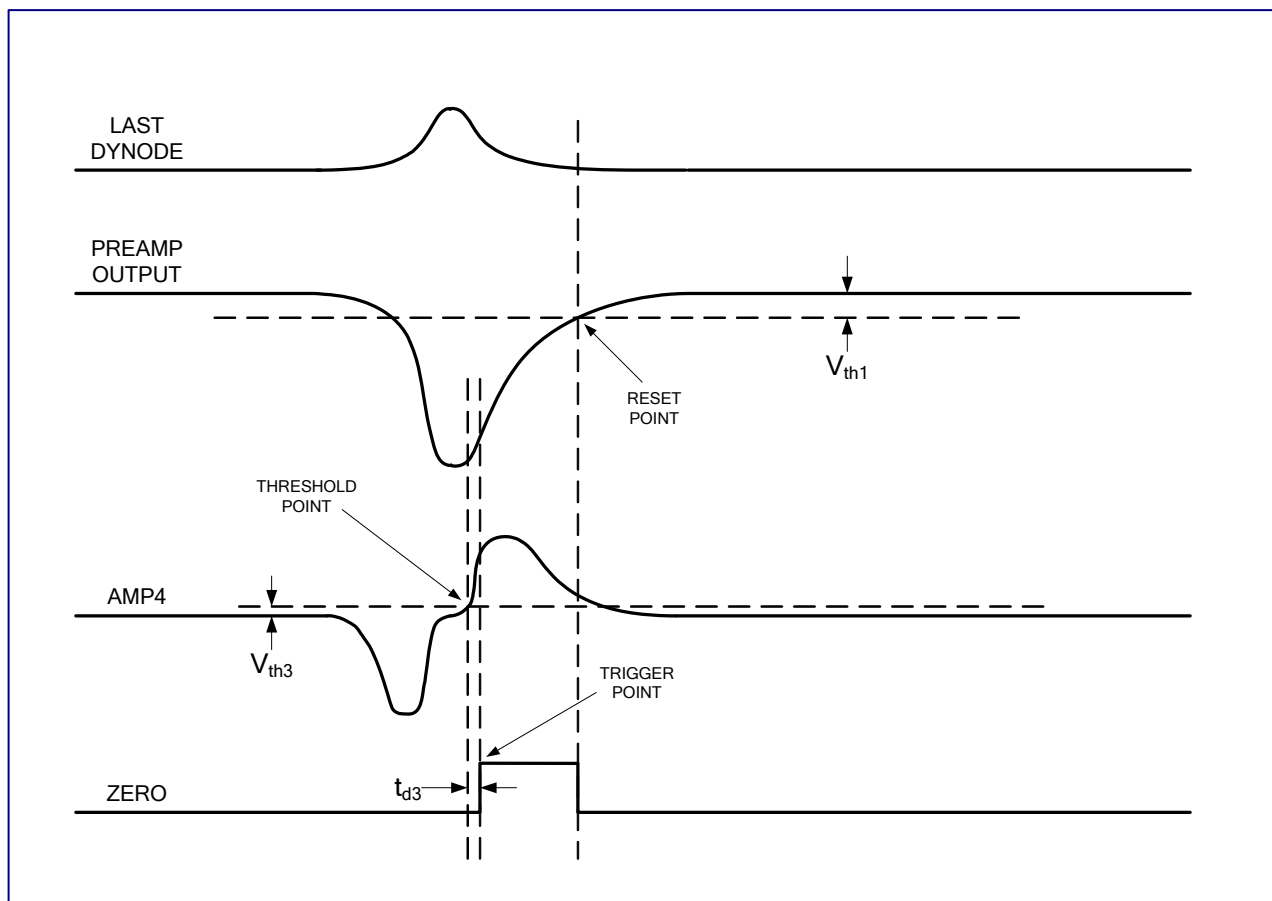


Figure 7: Zero Slope Discriminator Timing

Top and Bottom Views

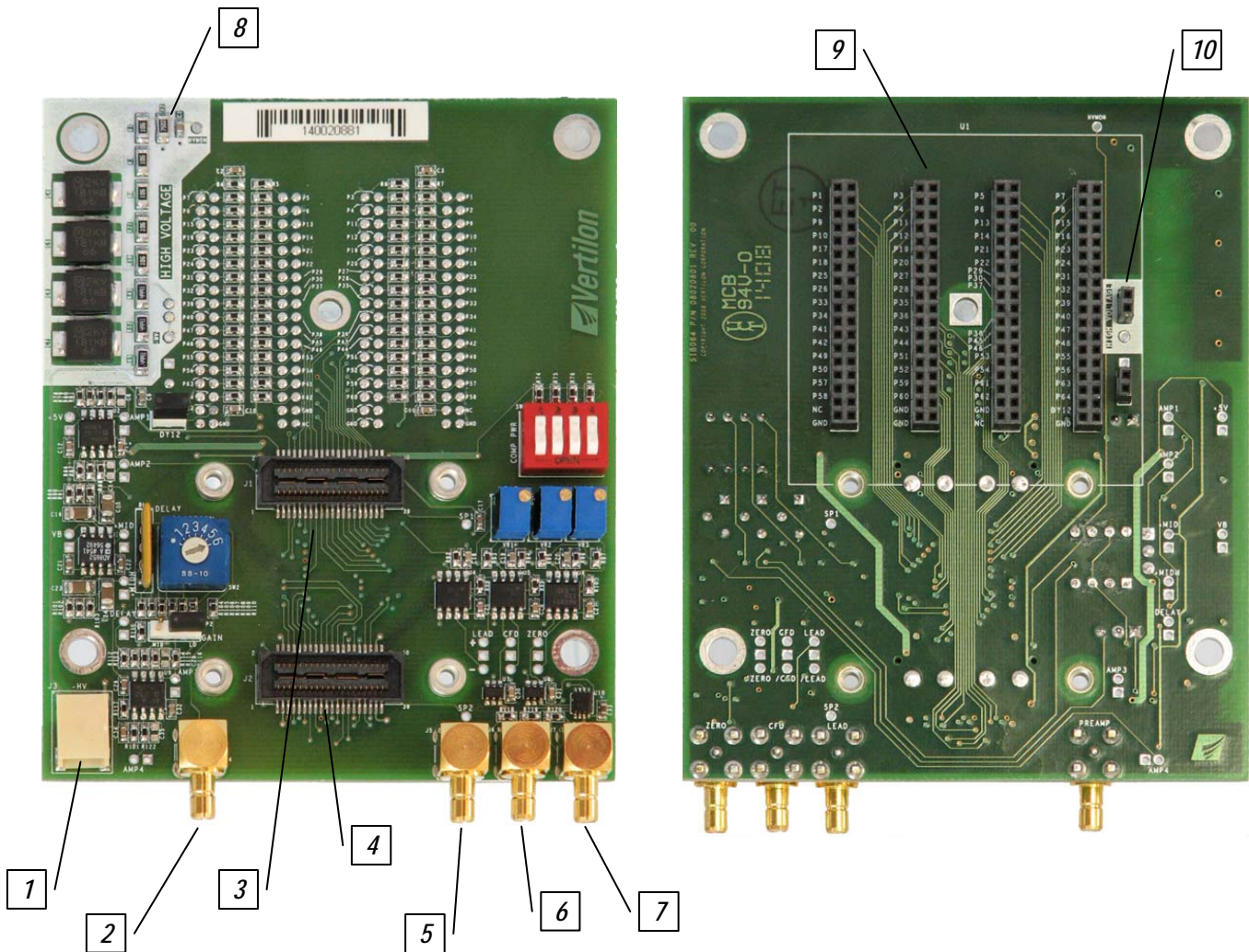


Figure 8: Top and Bottom Views

- | | |
|---|--|
| 1. High Voltage Input (J3) | 6. Constant Fraction Discriminator Output (J6) |
| 2. Preamplifier Output (J4) | 7. Zero Slope Discriminator Output (J7) |
| 3. Sensor Interface Board Connector (J1) | 8. High Voltage Section |
| 4. Sensor Interface Board Connector (J2) | 9. H850D Socket Connectors |
| 5. Leading Edge Discriminator Output (J5) | 10. H850D High Voltage Input |

Component Locations and Functions

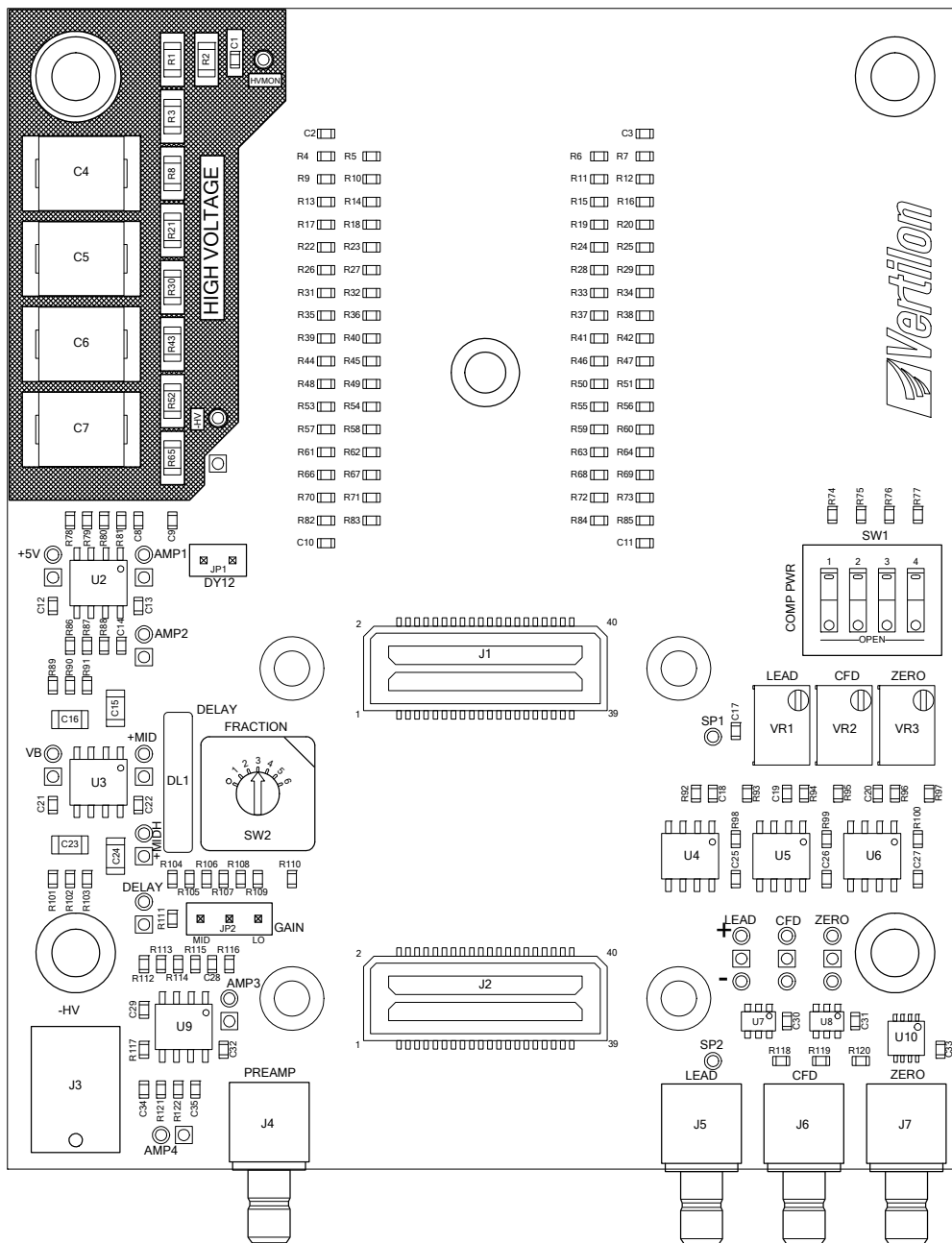


Figure 9: Component Locations and Functions

Name	Function	Description
J1	CHANNELS 1 - 32	Sensor interface board connector to SIB cable for channels 1 -32
J2	CHANNELS 33 - 64	Sensor interface board connector to SIB cable for channels 33 - 64
J3	-HV	Negative high voltage bias input
J4	PREAMP	Last dynode preamplifier output
J5	LEAD	Leading edge discriminator output
J6	CFD	Constant fraction discriminator output
J7	ZERO	Zero slope discriminator output

Table 2: Connectors

Name	Function	Description
JP1	DY12	Last dynode output to preamplifier input disconnect: remove jumper to disconnect
JP2	GAIN	Constant fraction discriminator gain: default equals "LO"
SW1-1	COMP PWR - LEAD	Power to leading edge discriminator: set to open to power down
SW1-2	COMP PWR - CFD	Power to constant fraction discriminator: set to open to power down
SW1-3	COMP PWR - ZERO	Power to zero slope discriminator: set to open to power down
SW1-4	COMP PWR -	Reserved
SW2	FRACTION	Constant fraction discriminator fraction: 0 = minimum, 6 = maximum
VR1	LEAD	Leading edge discriminator threshold: clockwise increases threshold
VR2	CFD	Constant fraction discriminator threshold: clockwise increases threshold
VR3	ZERO	Zero slope discriminator threshold: clockwise increases threshold
DL1	DELAY	Programmable delay element for constant fraction discriminator

Table 3: Jumpers, Switches, and Pots

Name	Description
+5V	Main +5V power to the SIB064 supplied by the PhotoniQ through SIB connectors J1 and J2.
VB	Anode bias and reference voltage to the SIB064 supplied by the PhotoniQ through SIB connectors J1 and J2.
+MID	Baseline voltage for last dynode signal processing chain. Nominally +2.5V.
+MIDH	Internal reference voltage.
-HV	PMT cathode bias. Warning: This is a high voltage point that can exceed negative 1500 volts.
HVMON	Highly attenuated version of -HV used for indirectly monitoring PMT cathode bias.
AMP1	Output of amplifier #1 in last dynode signal processing chain.
AMP2	Output of amplifier #2 in last dynode signal processing chain.
AMP3	Output of amplifier #3 in constant fraction discriminator.
AMP4	Output of amplifier #4 in zero slope discriminator.
DELAY	Output of constant fraction discriminator delay path. Reference to AMP2 to measure the delay.
LEAD	Leading edge discriminator comparator output, positive (+) and negative (-).
CFD	Constant fraction discriminator comparator output, positive (+) and negative (-).
ZERO	Zero slope discriminator comparator output, positive (+) and negative (-).
SP1	Reserved signal from the PhotoniQ on SIB connector J1.
SP2	Reserved signal from the PhotoniQ on SIB connector J2.

Table 4: Test Points

SIB Connector Pinout

The SIB064 connectors and cables are fully compatible with all Vertilon PhotoniQ systems. For applications utilizing data acquisition systems other than Vertilon's PhotoniQ series, the pinout for connectors J1 and J2 is provided in Table 5 as a reference.

J1				J2			
Signal Name	Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name	Pin #
VB	1	HVMON	2	VB	1	HVMON	2
GND	3	GND	4	GND	3	GND	4
P16	5	P32	6	P48	5	P64	6
P15	7	P31	8	P47	7	P63	8
P14	9	P30	10	P46	9	P62	10
P13	11	P29	12	P45	11	P61	12
P12	13	P28	14	P44	13	P60	14
P11	15	P27	16	P43	15	P59	16
P10	17	P26	18	P42	17	P58	18
P9	19	P25	20	P41	19	P57	20
P8	21	P24	22	P40	21	P56	22
P7	23	P23	24	P39	23	P55	24
P6	25	P22	26	P38	25	P54	26
P5	27	P21	28	P37	27	P53	28
P4	29	P20	30	P36	29	P52	30
P3	31	P19	32	P35	31	P51	32
P2	33	P18	34	P34	33	P50	34
P1	35	P17	36	P33	35	P49	36
GND	37	GND	38	GND	37	GND	38
SIBDAC	39	+5V	40	SIBDAC	39	+5V	40

Table 5: Sensor Interface Board (SIB) Connectors

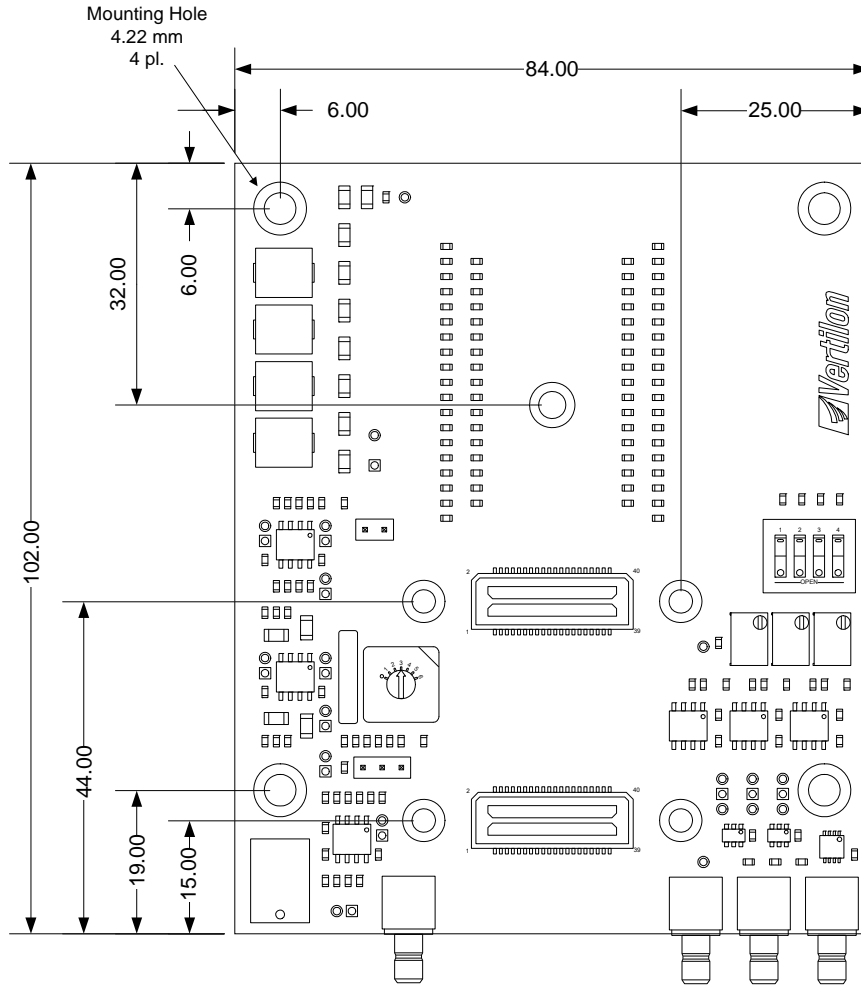
Power (+5V) supplied through pin 40 if PhotoniQ is not used

Pin 1 must be biased at +0.250V when not connected to a PhotoniQ

Pin 39 reserved for PhotoniQ and should be left unconnected if PhotoniQ is not used

Ground supplied through SIB cable shielding

Mechanical Information



ALL DIMENSIONS IN MILLIMETER

Figure 10: SIB064 Printed Circuit Board Dimensions



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