User Guide

SIB232
32 Channel PMT Interface Board
Hamamatsu H7260 series

Vertilon Corporation, 66 Tadmuck Road, Westford, MA 01886 / Tel: (978) 692-7070 / Fax: (978) 692-7010 / www.vertilon.com

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General Safety Precautions

Use Proper Power Source

The SIB232 is powered with a +5V power source directly from Vertilon's PhotoniQ multi-channel data acquisition systems. Use with any other power source may result in damage to the product.

Operate Inputs within Specified Range

To avoid electric shock, fire hazard, or damage to the product, do not apply a voltage to any input outside of its specified range.

Electrostatic Discharge Sensitive

Electrostatic discharges may result in damage to the SIB232. For these reasons, the SIB232 board is intended to be operated in a user's conductive instrument enclosure.

Do Not Operate in Wet or Damp Conditions

To avoid electric shock or damage to the product, do not operate in wet or damp conditions.

Do Not Operate in Explosive Atmosphere

To avoid injury or fire hazard, do not operate in an explosive atmosphere.

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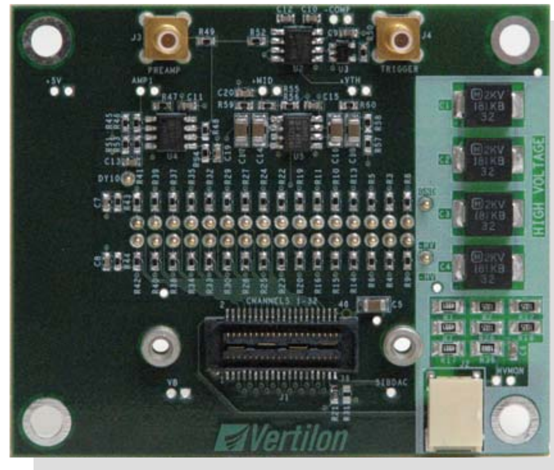
Product Overview

- Mounting board for Hamamatsu H7260 32 channel MAPMT
- Provides 32 channel interface to data acquisition systems
- Separate high voltage input for PMT cathode bias
- High speed preamplifier for last dynode output
- Leading edge discriminator with adjustable threshold
- 100% compatible with Vertilon's PhotoniQ multichannel DAQs
- No external power supply required



The SIB232 multianode photomultiplier tube interface board provides the mechanical and electrical connectivity between the Hamamatsu H7260 32 anode PMT and external signal processing electronics such as Vertilon's PhotoniQ multichannel data acquisition systems. The H7260 is mounted to the bottom side of the SIB232 through 35 socket pins that connect the PMT's 32 anode signals, high voltage input, and last dynode output to the board. The anode signals are routed to a connector located on the top of the board that connects to a specialized high density coaxial cable assembly. This arrangement allows the SIB232 to be conveniently mounted directly into the user's optical setup with the PMT facing outward from the bottom of the board and the sensor interface board (SIB) cable exiting from the top. The SIB cable carries the 32 anodes from the H7260 to the PhotoniQ where the charge from each is separately integrated, digitized, and sent to a PC for display or further signal processing. The negative high voltage bias to the PMT's cathode is supplied directly from the PhotoniQ on a high voltage cable to a dedicated connector on the SIB232. For applications utilizing the last dynode output of the H7260, the SIB232 includes a two stage high speed preamplifier and a leading edge discriminator whose outputs are available on SMB connectors. The discriminator's threshold is fully adjustable using the PhotoniQ. When critical timing and triggering are required, the on-board discriminator can be bypassed and the preamp output can be connected to a separate high performance external discriminator.

The various functions on the SIB232 are described in greater detail on the following pages. When necessary, refer to the functional block diagram shown in Figure 1 below.

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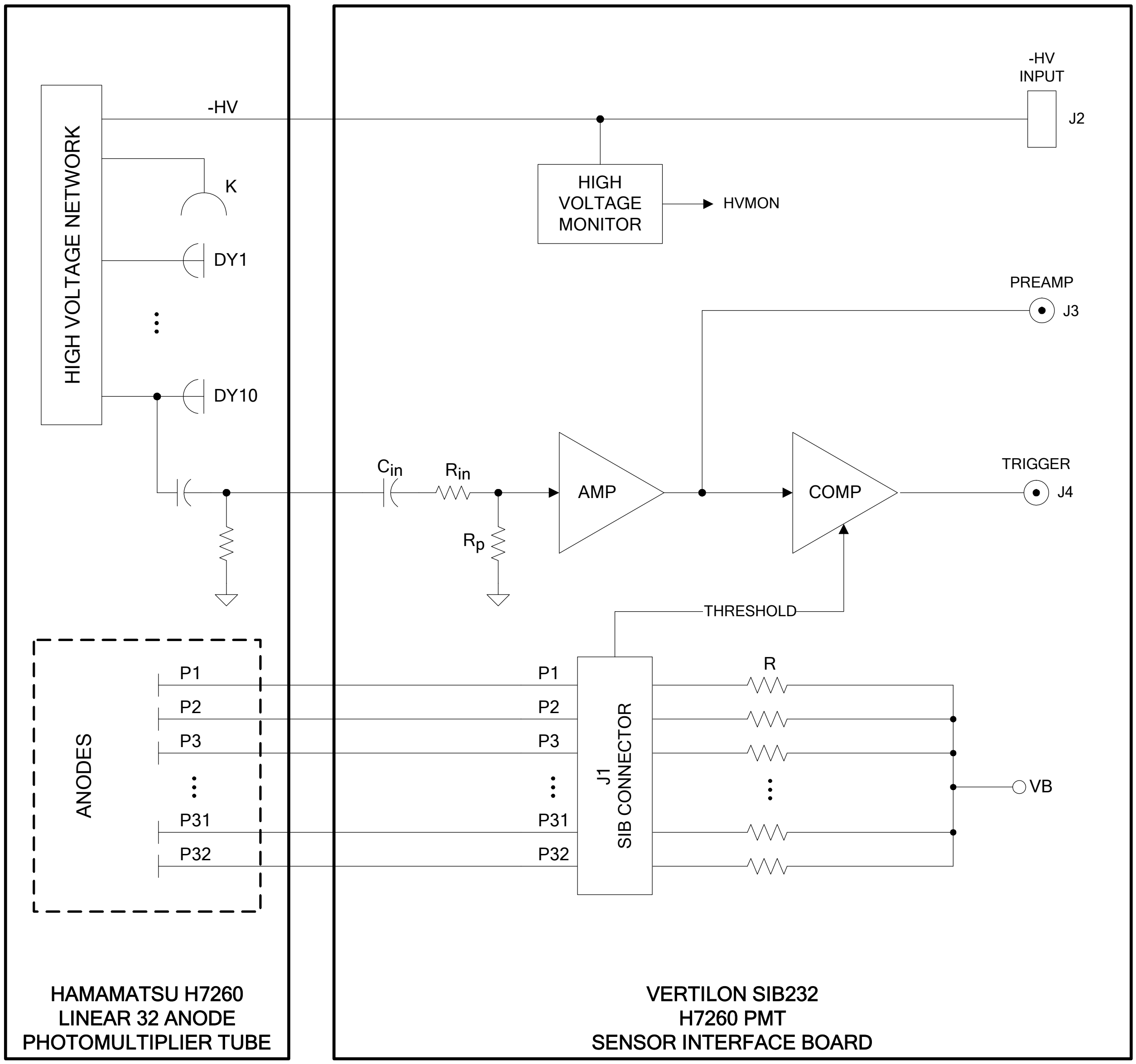

Figure 1: Functional Block Diagram

Specifications

(V_{supply} = +5.0V, T_A = +25C, unless otherwise noted)

Description	Sym	Min	Typ	Max	Units	Notes
HIGH VOLTAGE						
High Voltage Input Load Resistance			40		MΩ	Measured at high voltage input connector, J2
HVMON to High Voltage Input Ratio			0.0025			±10%
ANODE CIRCUITS						
Quantity	P1 - P32		32			
Input Resistance	R		2.2		MΩ	This resistor value is open for SIB232D version
Input Bias Voltage	VB		+0.250		V	Detector bias voltage supplied from PhotoniQ data acquisition system
LAST DYNODE PREAMPLIFIER						
Input Coupling Capacitance	C_{in}		0.1		uF	
Input Resistance	R_{in}		50		Ω	
Input Parallel Resistance	R_p		500		Ω	
1^{ST} Stage Gain	A1		13.4		dB	
2^{nd} Stage Inverting Gain	A2		6		dB	V_{in} is a triangular pulse (18 nsec rise time, 30 nsec fall time) applied to last dynode preamplifier input (DY10).
2^{nd} Stage Output Impedance			50		Ω	Measured at preamplifier output, J3
LEADING EDGE DISCRIMINATOR						
Threshold Adjustment	V_{th}	-25		0	mV	Referenced to baseline level at comparator input
Threshold to Output Delay (V_{in}=30mV)	t_d		6	9	nsec	Output on connector, J4
Time Walk (V_{in}: 3mV to 150mV)			-20		nsec	V_{in} is a triangular pulse (18 nsec rise time, 30 nsec fall time) applied to last dynode preamplifier input (DY10). Threshold (V_{th}) set to 25mV below the baseline.
Jitter (V_{in}: 10mV)			500		psec	
Output Impedance			50		Ω	
Logic High Output Level	V_{OH}	+4.3	+4.8		V	(I_{OH} = -32mA)
Logic Low Output Level	V_{OL}		+0.2	+0.6	V	(I_{OL} = 32mA)
POWER						
Supply Voltage	V_{supply}	+4.9	+5.0	+5.1	V	
Supply Current	I_{supply}		45		mA	
DIMENSIONS						
Width	W		76		mm	
Length	L		64		mm	
Thickness	T		1.6		mm	(printed circuit board only)

Table 1: Specifications

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Typical Setup

In a typical fluorescence detection setup, the Hamamatsu H7260 PMT is plugged into the SIB232 sensor interface board which in turn connects using a SIB cable to a Vertilon PhotoniQ IQSP480 or IQSP580 multichannel data acquisition system. An optical grating on the front surface of the PMT filters the incoming fluorescence signal such that each of the PMTs 32 outputs is sensitive to a particular band of ultraviolet light. Events are acquired by the PhotoniQ when triggered by either an external source such as a pulsed laser excitation, or by the SIB232's on-board discriminator connected to the PMT's last dynode output. Each trigger causes the PhotoniQ to integrate and digitize the 32 charge signals from the H7260 and output them in a data packet over a USB connection to the PC. The PhotoniQ also supplies the PMT with a negative high voltage bias of up to -925 volts through a specialized high voltage cable.

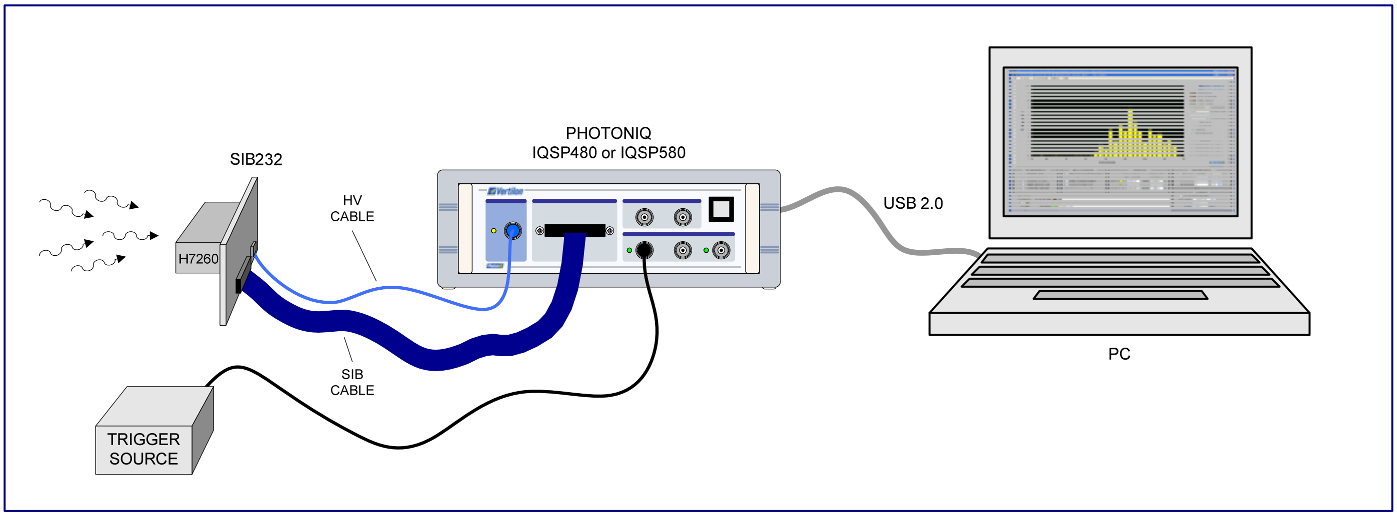

Figure 2: Typical Fluorescence Detection Setup

High Voltage Interface

The SIB232 employs the interface circuit shown below between the high voltage input connector, J2, and the high voltage input to the H7260. The monitor output (HVMON) allows the high voltage cathode bias for the PMT to be indirectly monitored at a reduced voltage level. Voltage readings at the monitor point should be scaled by a factor of 400. Calibration of the scale factor may be required.

Warning: The high voltage section of the SIB232 contains signals at voltage levels that can exceed negative 1500 volts. Never touch a component or signal in this area.

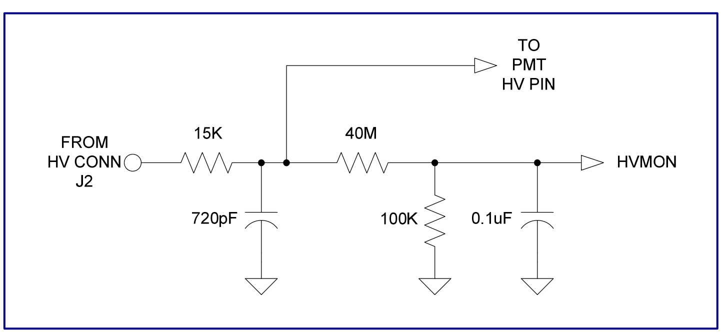

Figure 3: PMT High Voltage Interface Circuit

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Photomultiplier Tube Anode Circuits

The 32 anode signals (P1 – P32) from the H7260 PMT are routed directly on the SIB232 to a specialized connector (J1) referred to as a sensor interface board (SIB) connector. The SIB connector mates to a proprietary low-noise, high density SIB cable assembly that carries the 32 anode signals on coaxial connections to a Vertilon PhotoniQ 32 channel PMT data acquisition system. Depending on the required speed and dynamic range, either a PhotoniQ IQSP480 high dynamic range system or an IQSP580 high speed system can be used as the main data acquisition unit. To minimize the possibility of damage due to ESD, the H7260 anodes each have a 2.2 Mohm shunt resistor to a common low impedance point. This point is biased at a voltage equal to the bias voltage (VB) of the charge integrating transimpedance amplifiers on the PhotoniQ so that the anodes can be DC coupled to them. Figure 4 below illustrates the equivalent circuit as seen by each PMT anode. For ultra-low current applications, the model SIB232D is available which does not include the 2.2 Mohm resistors.

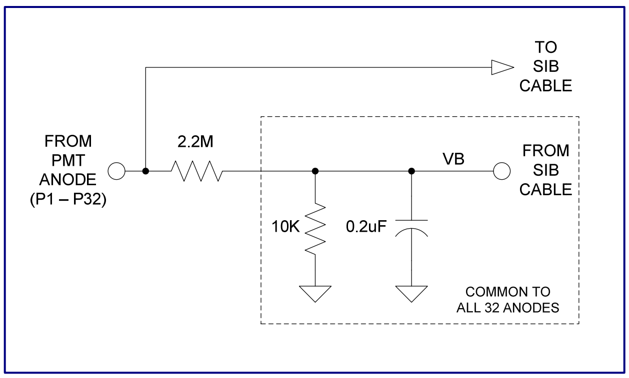

Figure 4: Anode Circuit

Last Dynode Preamplifier

This last dynode preamplier is an inverting, AC-coupled, two-stage configuration whose input is designed for small positive voltage pulses from the last dynode (DY10) of the H7260. The preamplifier's output can be further processed by the leading edge discriminator on the SIB232 to generate trigger signals in sync with the pulse on the last dynode. For specialized applications requiring external discrimination of the last dynode signal, the preamplifier output is available on SMB connector, J3.

Leading Edge Discriminator

The leading edge discriminator is a simple timing circuit that generates a trigger signal when a charge pulse on the last dynode output from the H7260 PMT exceeds a user-defined threshold. It is implemented using a high speed comparator connected to the output of the last dynode preamplier. Referring to Figure 5, negative going pulses from the preamplifier are compared to a threshold that is adjusted using the sensor interface board DAC on the PhotoniQ. Since the signal baseline for the SIB264 discriminator is nominally +2.5V, the threshold should be adjusted slightly below this baseline voltage. A logic high is generated on the comparator output (SMB connector, J4) after a small delay (t_d) from when the pulse first crosses the threshold, V_{th}. The comparator switches back to a logic low when the pulse crosses the threshold from the opposite direction as it returns back to the baseline level. Because the trigger point is sensitive to the pulse height, this discriminator is typically used in applications that do not require precision timing. When not used, the leading edge discriminator should be disabled by setting the threshold on the PhotoniQ to zero volts.

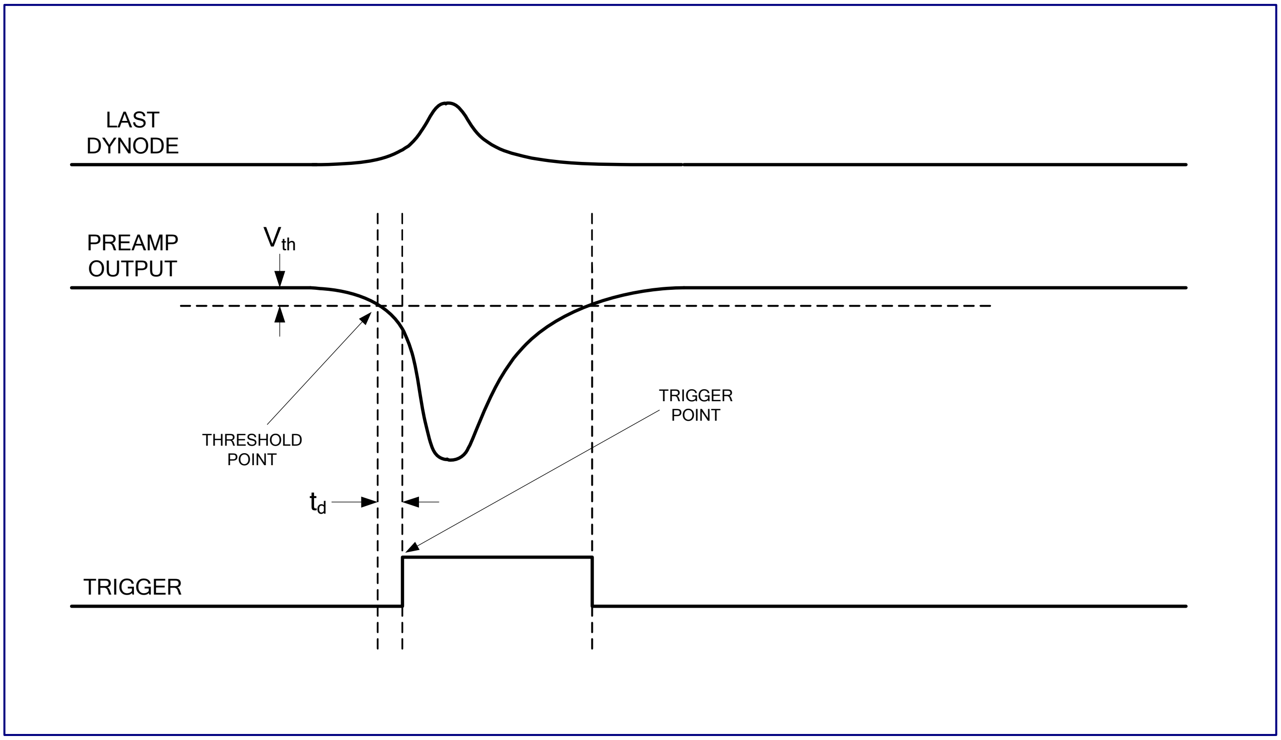

Figure 5: Leading Edge Discriminator Timing

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Top and Bottom Views

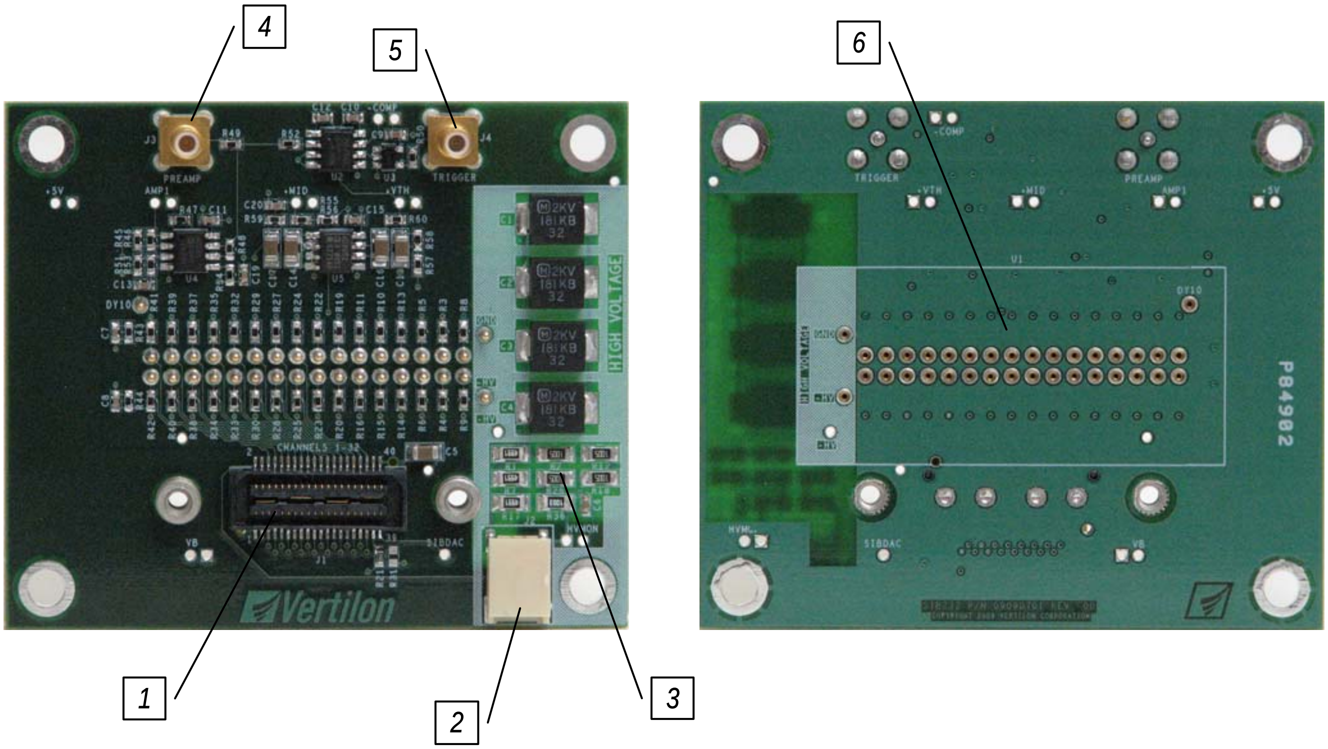

Figure 6: Top and Bottom Views

1. Sensor Interface Board Connector (J1)
2. High Voltage Input (J2)
3. High Voltage Section
4. Preamp Output (J3)
5. Discriminator Output (J4)
6. H7260 Socket Connectors

Name	Function	Description
J1	CHANNELS 1 - 32	Sensor interface board connector to SIB cable for channels 1 -32
J2	-HV	Negative high voltage bias input
J3	PREAMP	Last dynode preamplifier output
J4	TRIGGER	Leading edge discriminator output

Table 2: Connectors

Name	Description
+5V	Main +5V power to the SIB232 supplied by the PhotoniQ through SIB connector J1.
VB	Anode bias and reference voltage to the SIB232 supplied by the PhotoniQ through SIB connector J1.
+MID	Baseline voltage for last dynode signal processing chain. Nominally +2.5V.
-HV	PMT cathode bias. **Warning: This is a high voltage point that can exceed negative 1500 volts.**
HVMON	Highly attenuated version of –HV used for indirectly monitoring PMT cathode bias.
AMP1	Output of 1st stage amplifier in last dynode signal processing chain.
SIBDAC	Discriminator threshold control voltage from the PhotoniQ on SIB connector J1.
+VTH	Threshold voltage to leading edge discriminator.
-COMP	Leading edge discriminator comparator negative output.

Table 3: Test Points

SIB Connector Pinout

The SIB232 connectors and cables are fully compatible with all Vertilon PhotoniQ systems. For applications utilizing data acquisition systems other than Vertilon's PhotoniQ series, the pinout for connector J1 is provided in Table 4 as a reference.

J1			
Signal Name	Pin #	Signal Name	Pin #
VB	1	HVMON	2
SIB_DIN	3	SIB_CLK	4
P16	5	P32	6
P15	7	P31	8
P14	9	P30	10
P13	11	P29	12
P12	13	P28	14
P11	15	P27	16
P10	17	P26	18
P9	19	P25	20
P8	21	P24	22
P7	23	P23	24
P6	25	P22	26
P5	27	P21	28
P4	29	P20	30
P3	31	P19	32
P2	33	P18	34
P1	35	P17	36
SIB_DOUT	37	SIB_SYNC	38
SIBDAC	39	+5V	40

Table 4: Sensor Interface Board (SIB) Connector Pinout

Power (+5V) supplied through pin 40 if PhotoniQ is not used
Pin 1 must be biased at +0.250V when not connected to a PhotoniQ
Pin 39 controls threshold to discriminator if PhotoniQ is not used
Pins 3, 4, 37, 38 used by PhotoniQ and should be left unconnected
Ground supplied through SIB cable shielding

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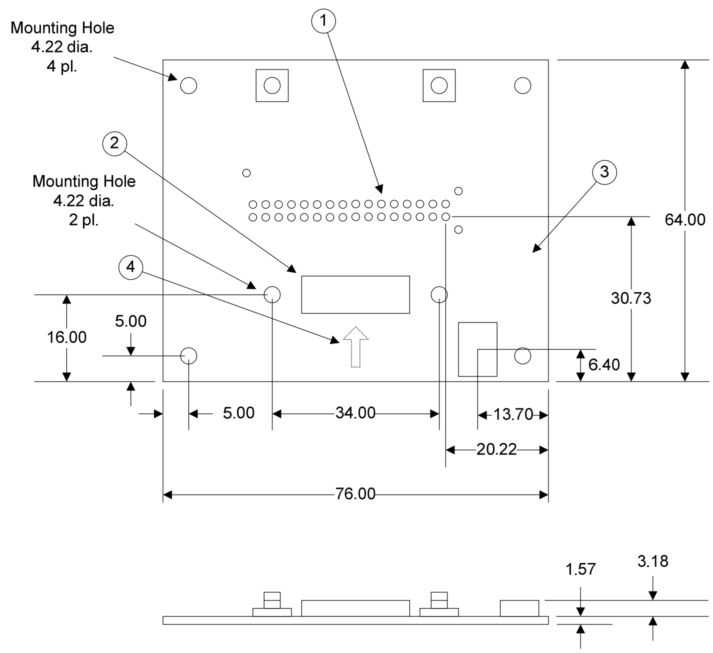
Mechanical Information



Notes: Item #1 is PMT socket pins. PMT connects to bottom side of PCB.
Item #2 is SIB connector. Height is 9.65mm with cable installed.
Item #3 is high voltage cable connector.
Item #4 indicates cable entry direction.
All dimensions in millimeter.

Figure 7: SIB232 Printed Circuit Board Dimensions

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